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(71) Applicant: **VICTOR CO OF JAPAN LTD**
(72) Inventor: **IWATA KAZUMI**

(54) BUFFER MEMORY OF INFORMATION RECORDING AND REPRODUCING DEVICE

(57) Abstract:

PURPOSE: To provide the buffer memory which is simple in constitution and fast in operation speed.

CONSTITUTION: Address signals of write column and row addresses, read column and row addresses, etc., are multiplexed by an address multiplexer 40 on a time-division basis and supplied to a D-RAM 31, and data are written in the form of digital data by every data amount of bits obtained by raising power to the (m)th with respect to 2 in relation of $n \leq m$,, where (n) is the number of bits of the row address. When a writing inhabited period is changed into a writing allowed period, the count value of a write row address counter 35 is preset to zero. The write row address signal is a write row address signal in the period wherein the data are allowed to be written in the D-RAM 31 and a refresh address signal in the period wherein the data are inhibited from being written. In the data writing allowed period, sequential memory cycles are generated through writing operation and reading operation, and in the data writing inhibited period, sequential memory cycles are generated through refreshing operation and the reading operation.